

[illegible]

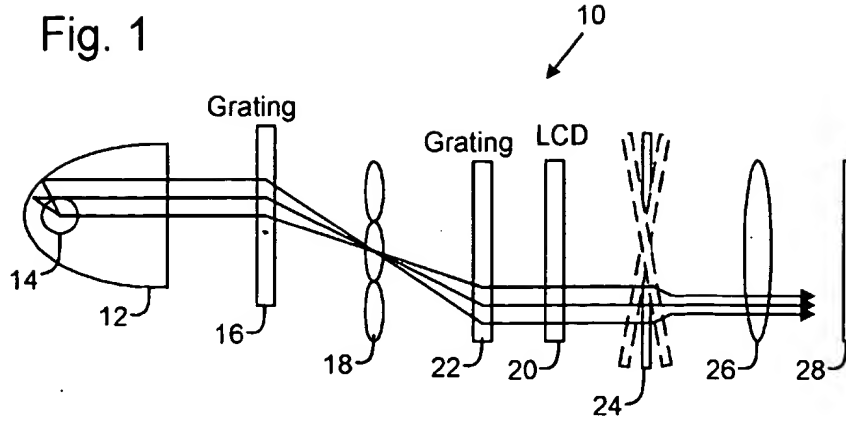


Fig. 5

LCD (58)

Columns x

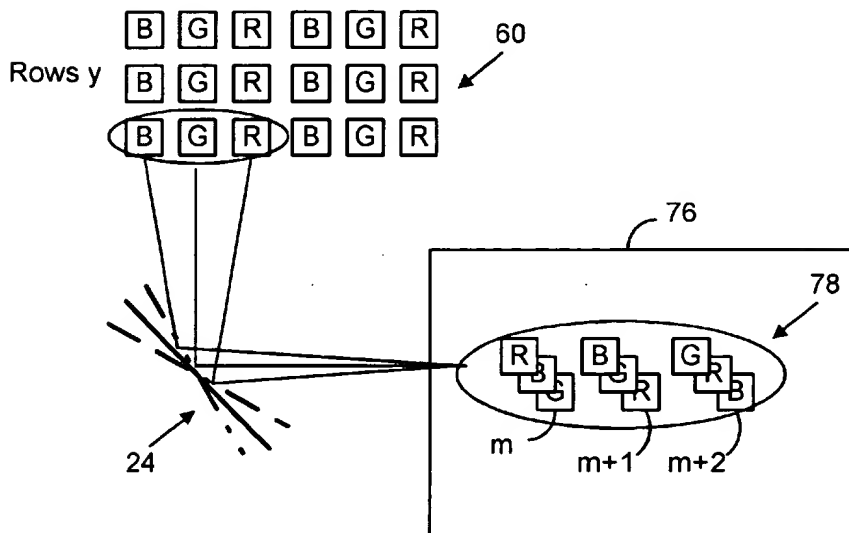


Fig. 2 - Prior Art

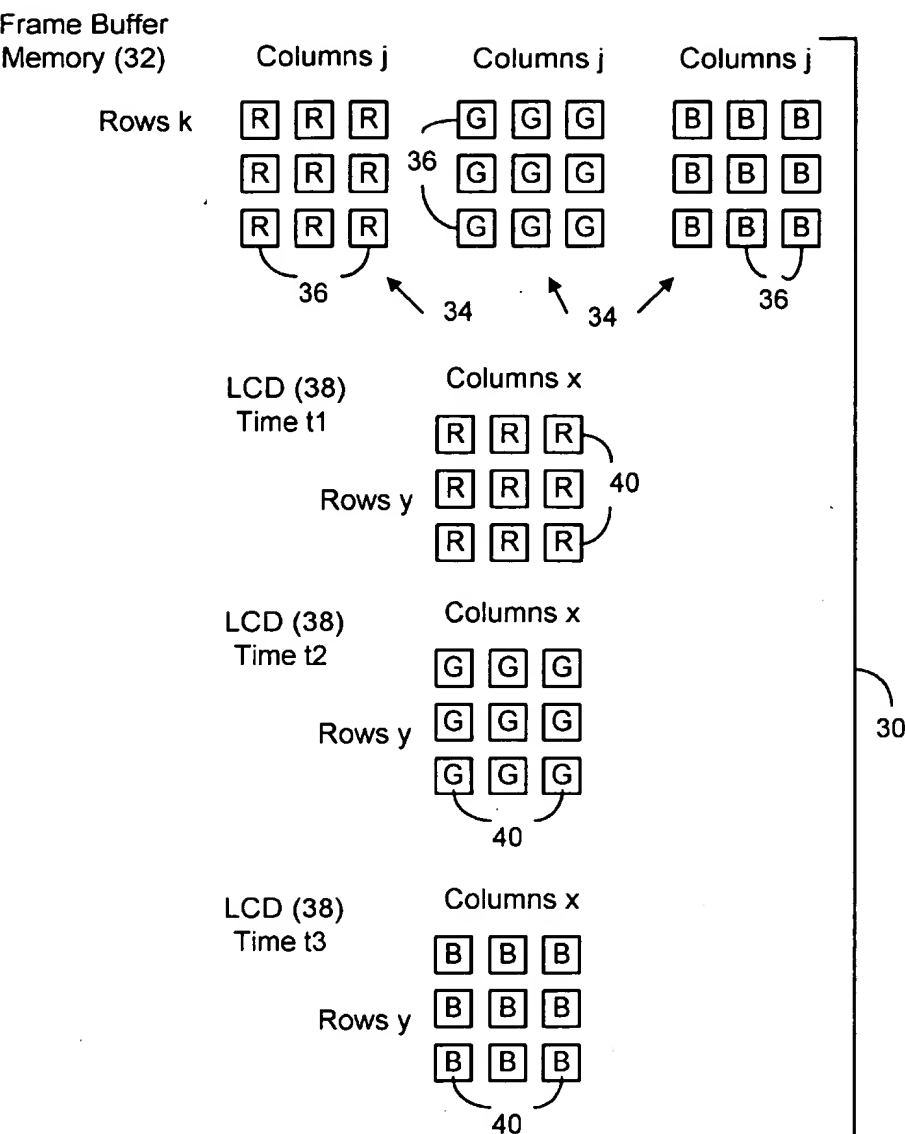
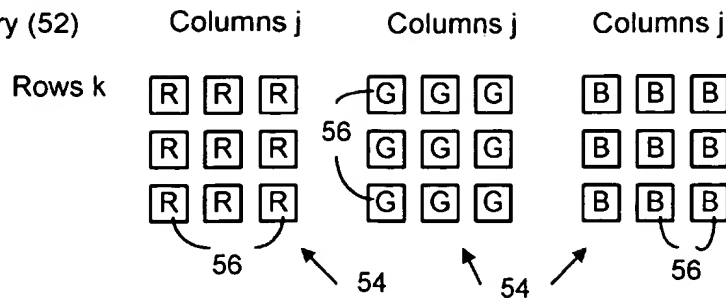
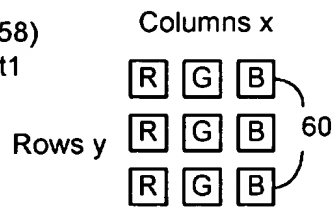


Fig. 3

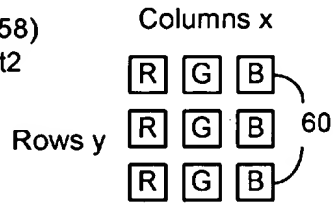
Frame Buffer
Memory (52)



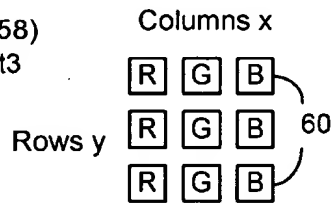
LCD (58)
Time t1



LCD (58)
Time t2



LCD (58)
Time t3



50

Fig. 4

Frame Buffer
Memory (52)

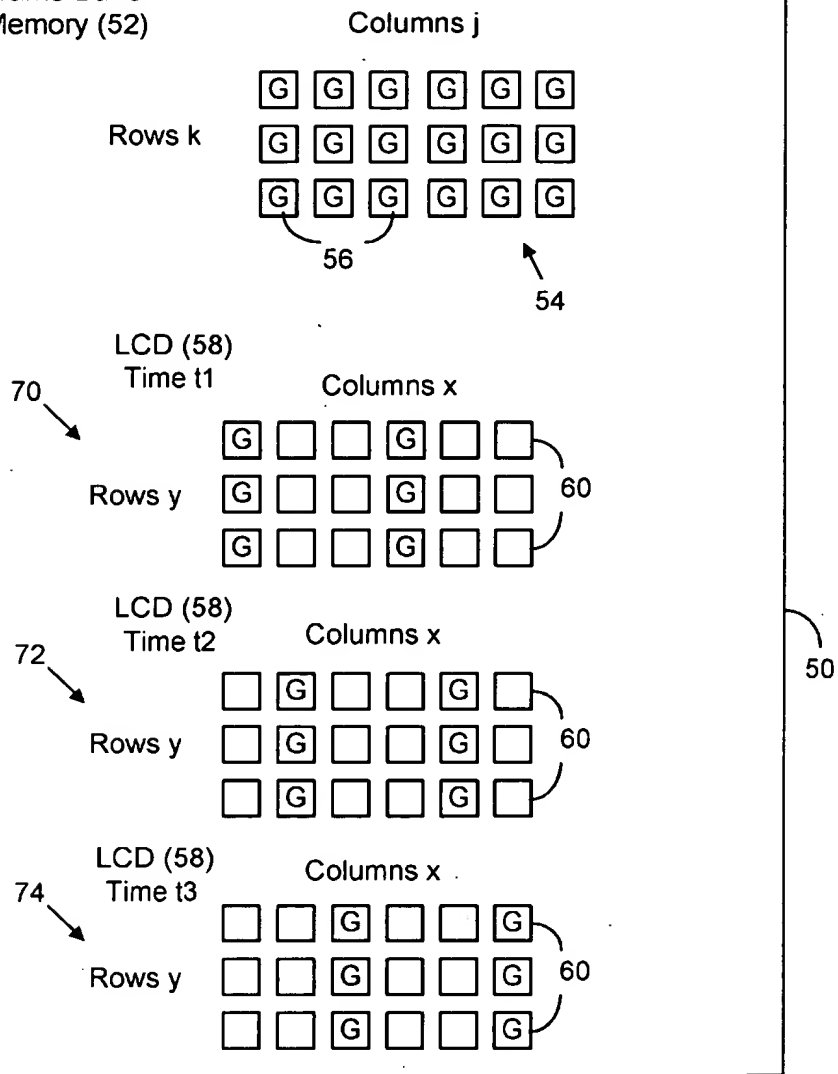


Fig. 6

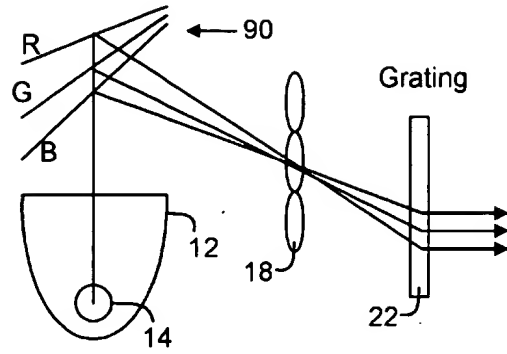


Fig. 7

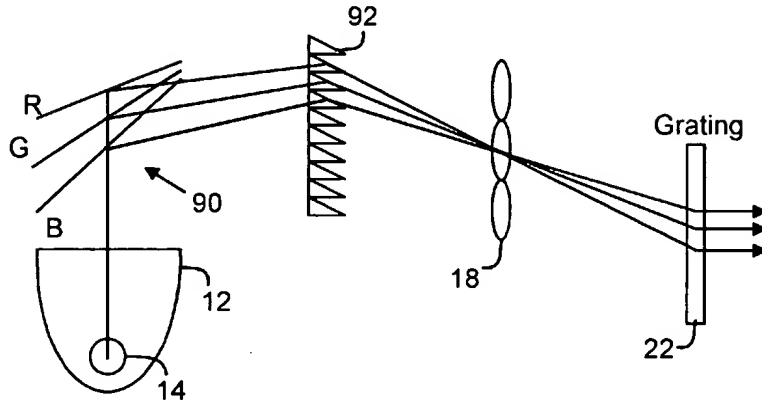


Fig. 8

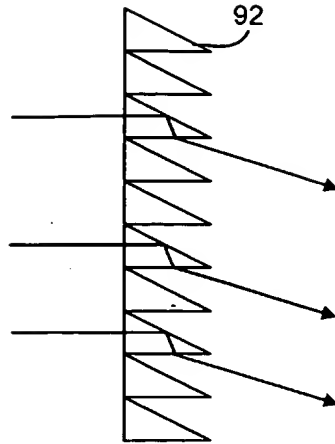


Fig. 9

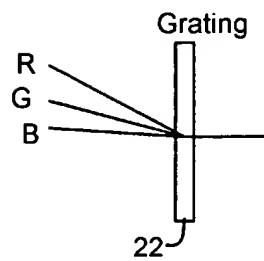


Fig. 10

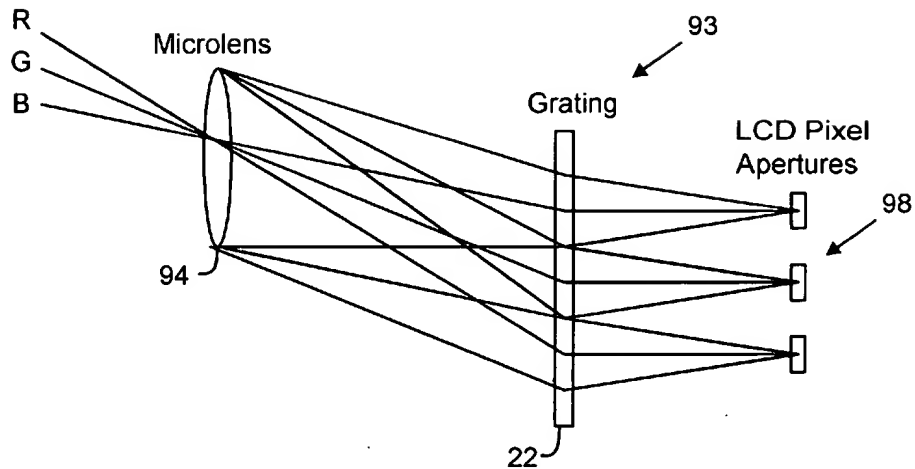


Fig. 11

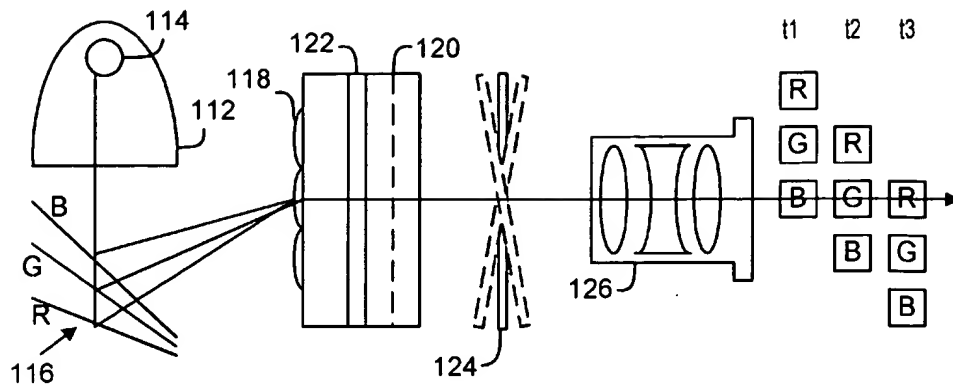


Fig. 12

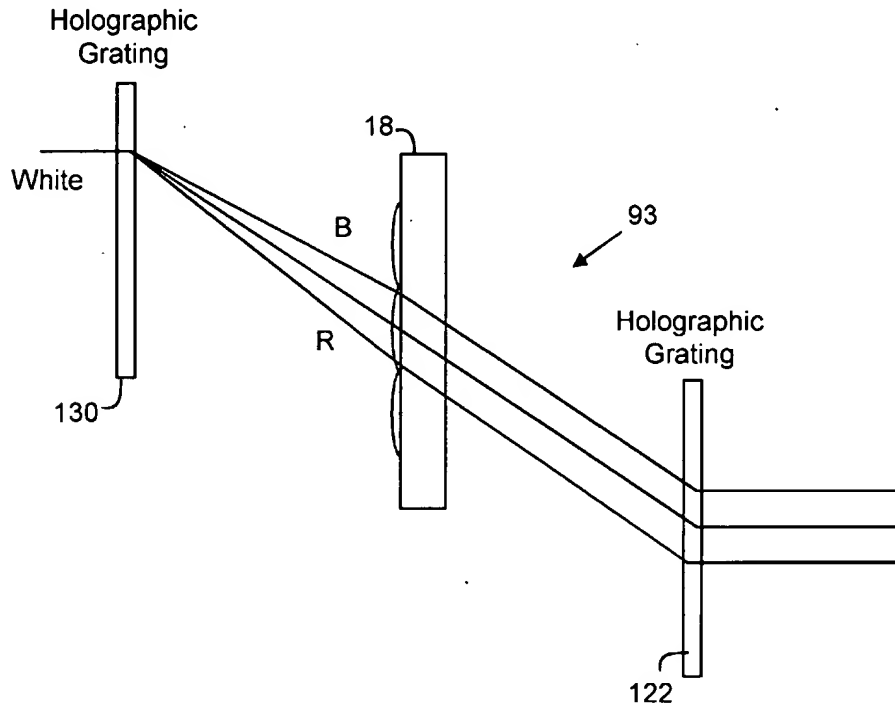


Fig. 13

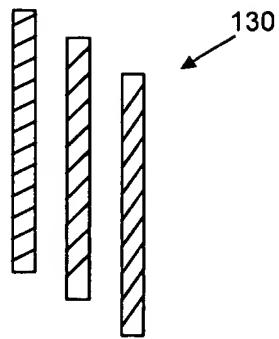


Fig. 14

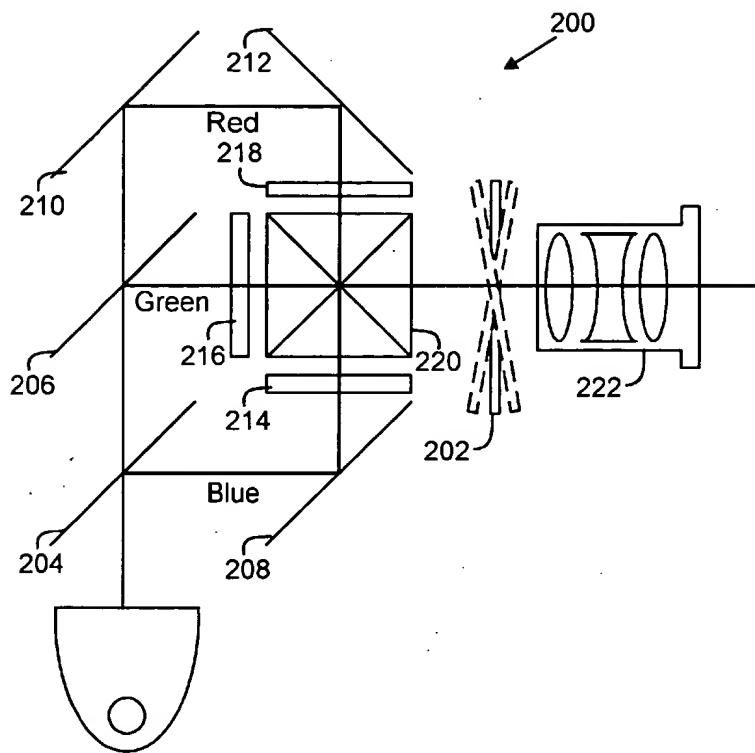


Fig. 15

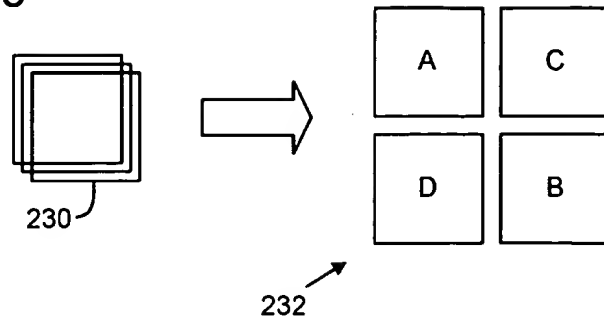


Fig. 16

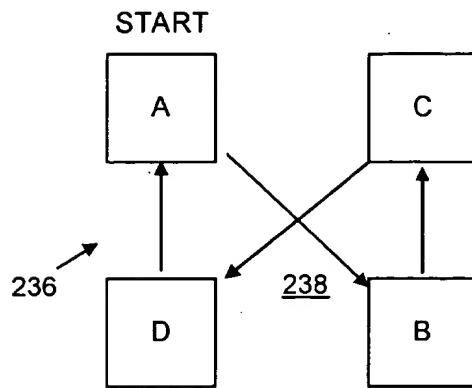


Fig. 17

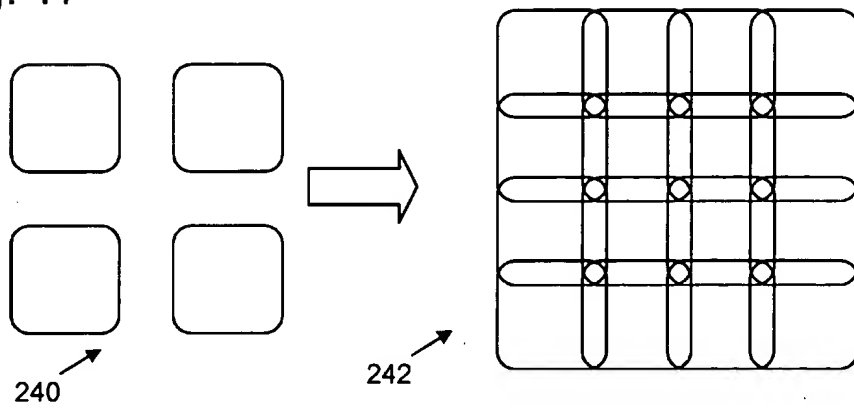


Fig. 15

Fig. 18

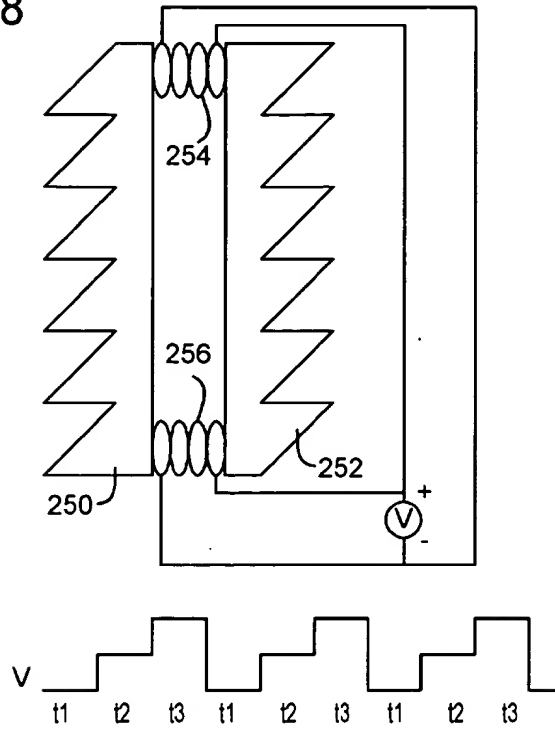


Fig. 19

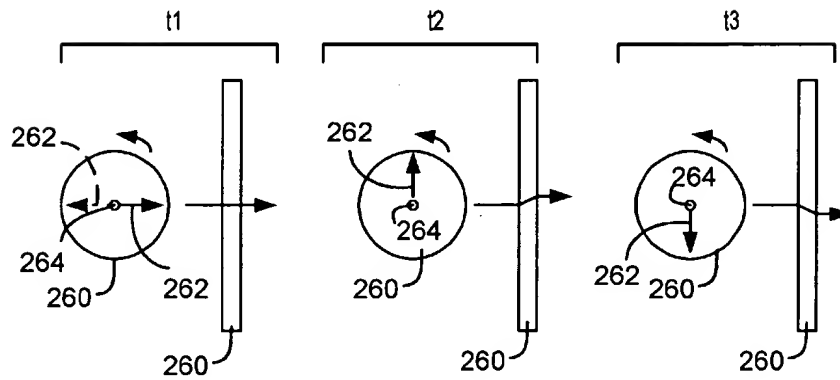


Fig. 20

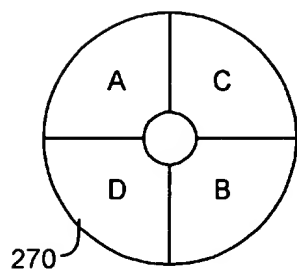


Fig. 21

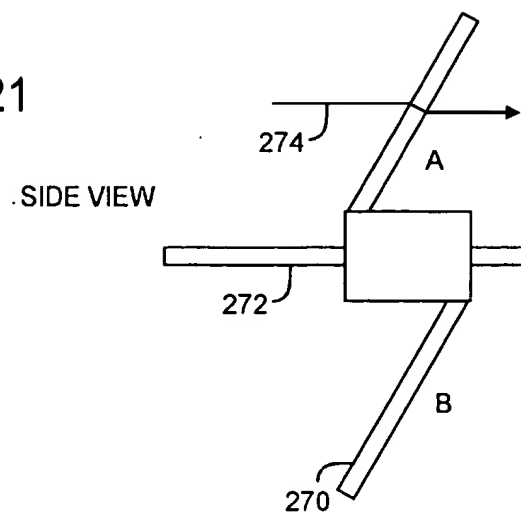


Fig. 22

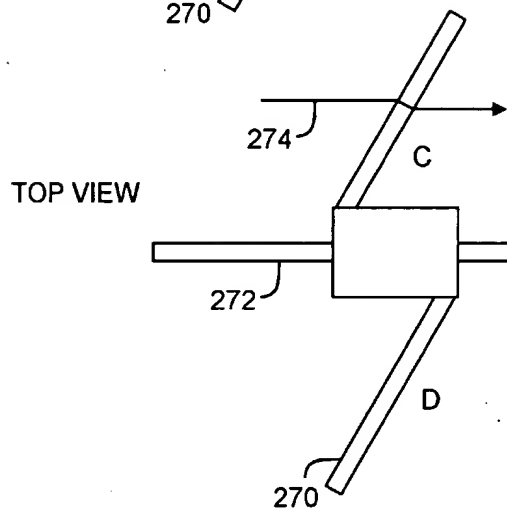


Fig. 23

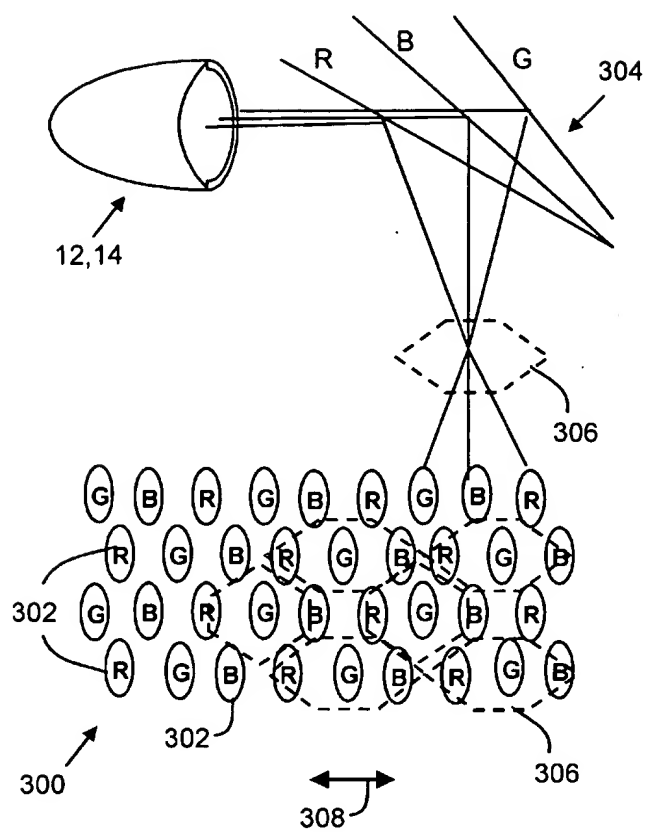


Fig. 24

